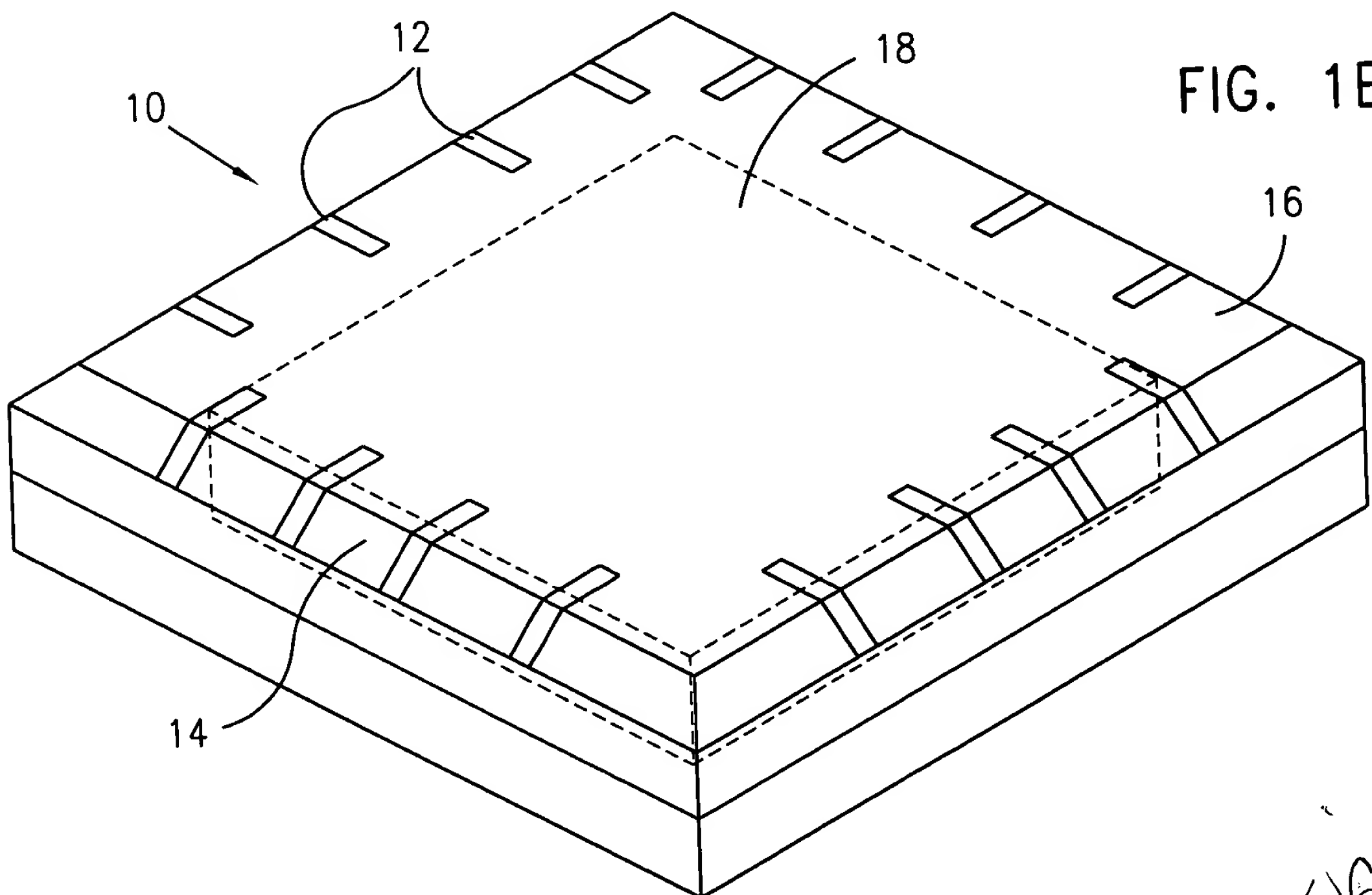
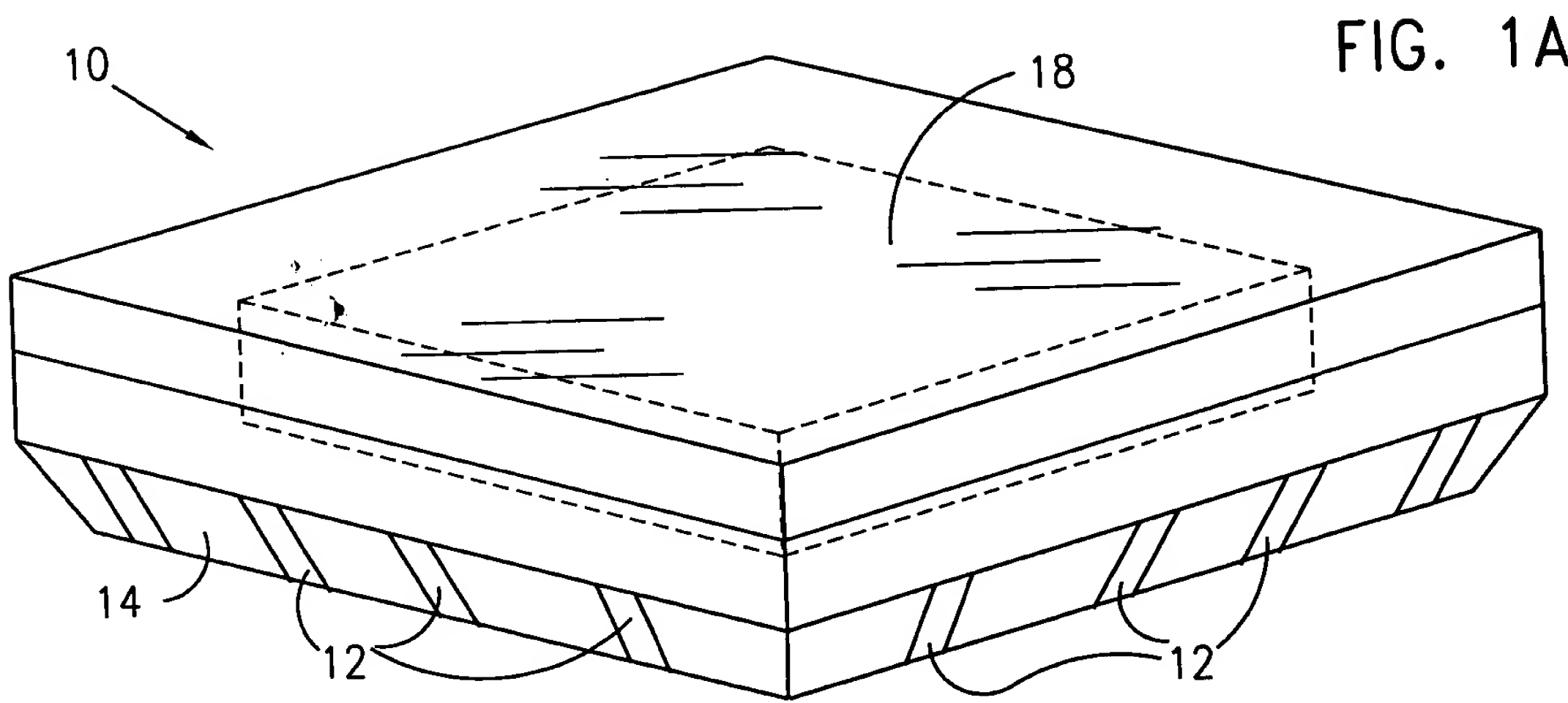


10/18



FIGS. 45

FIG. 2A

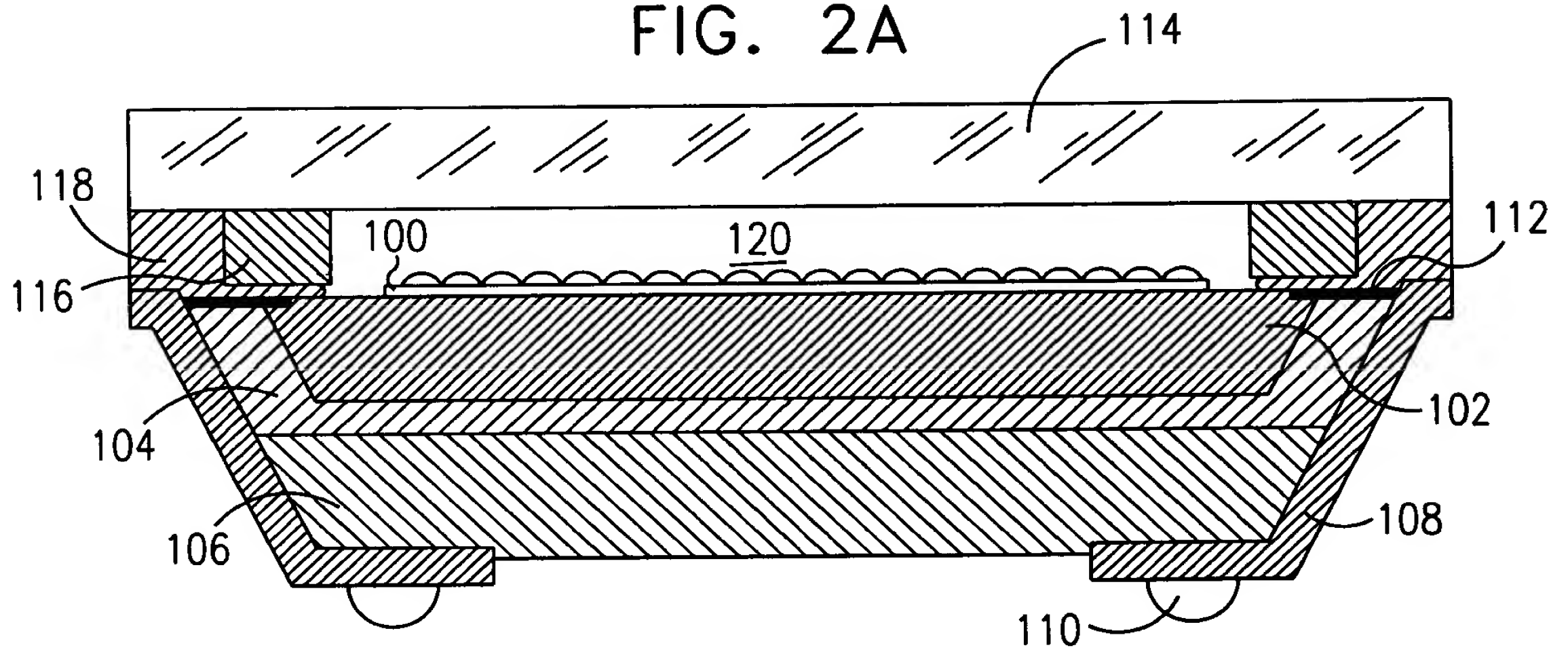


FIG. 2B

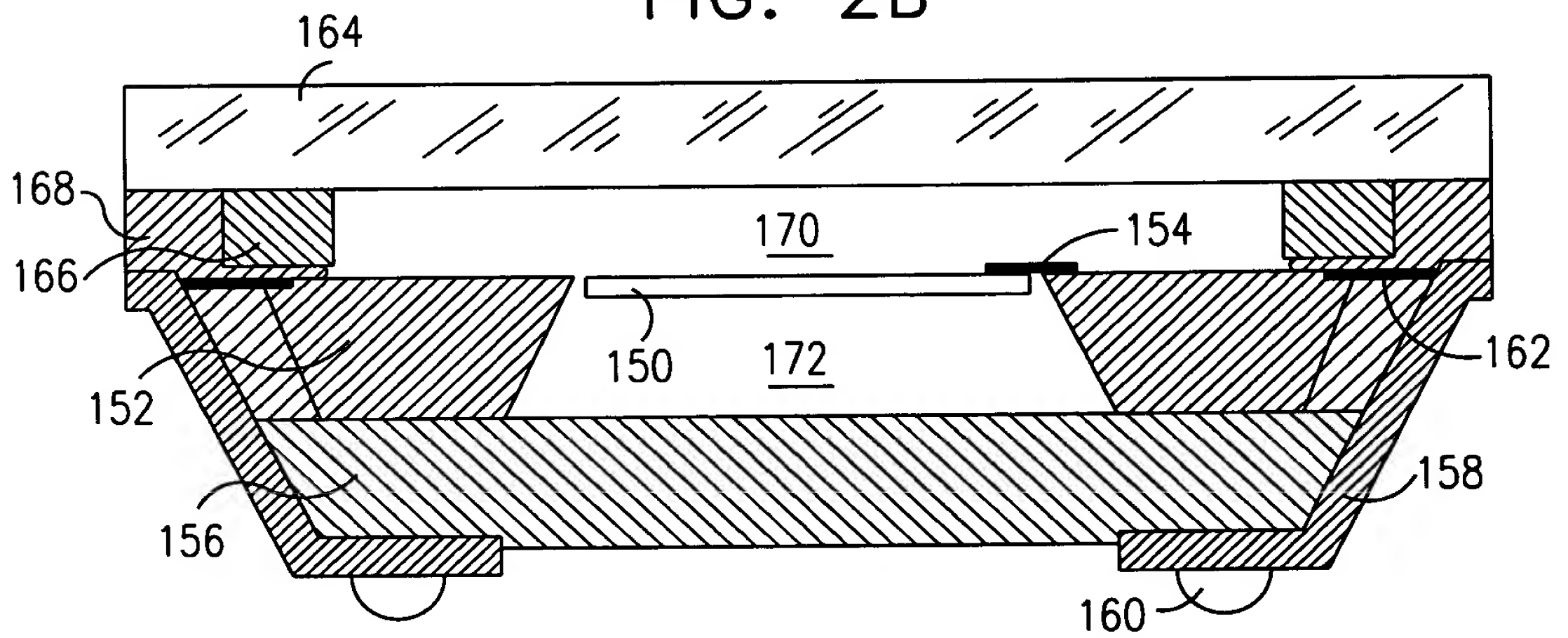


FIG. 2C

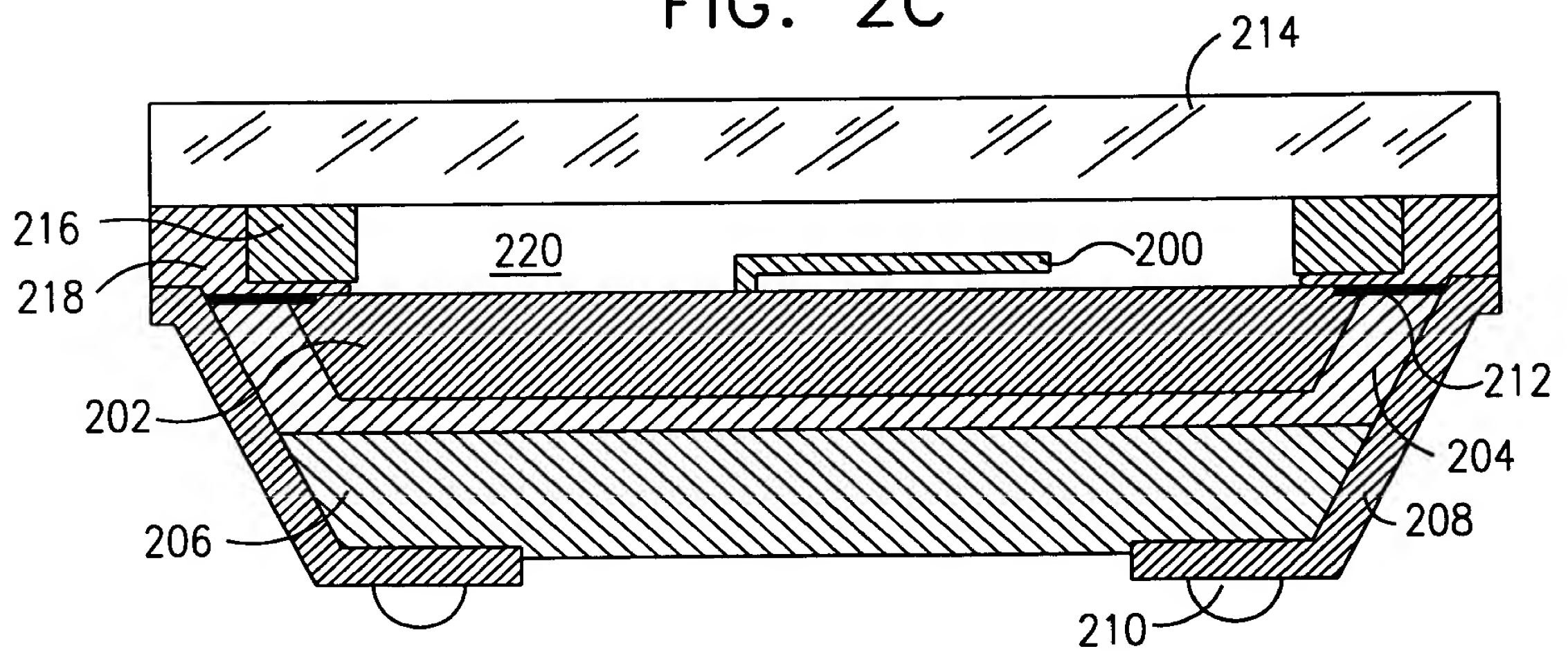


FIG. 2D

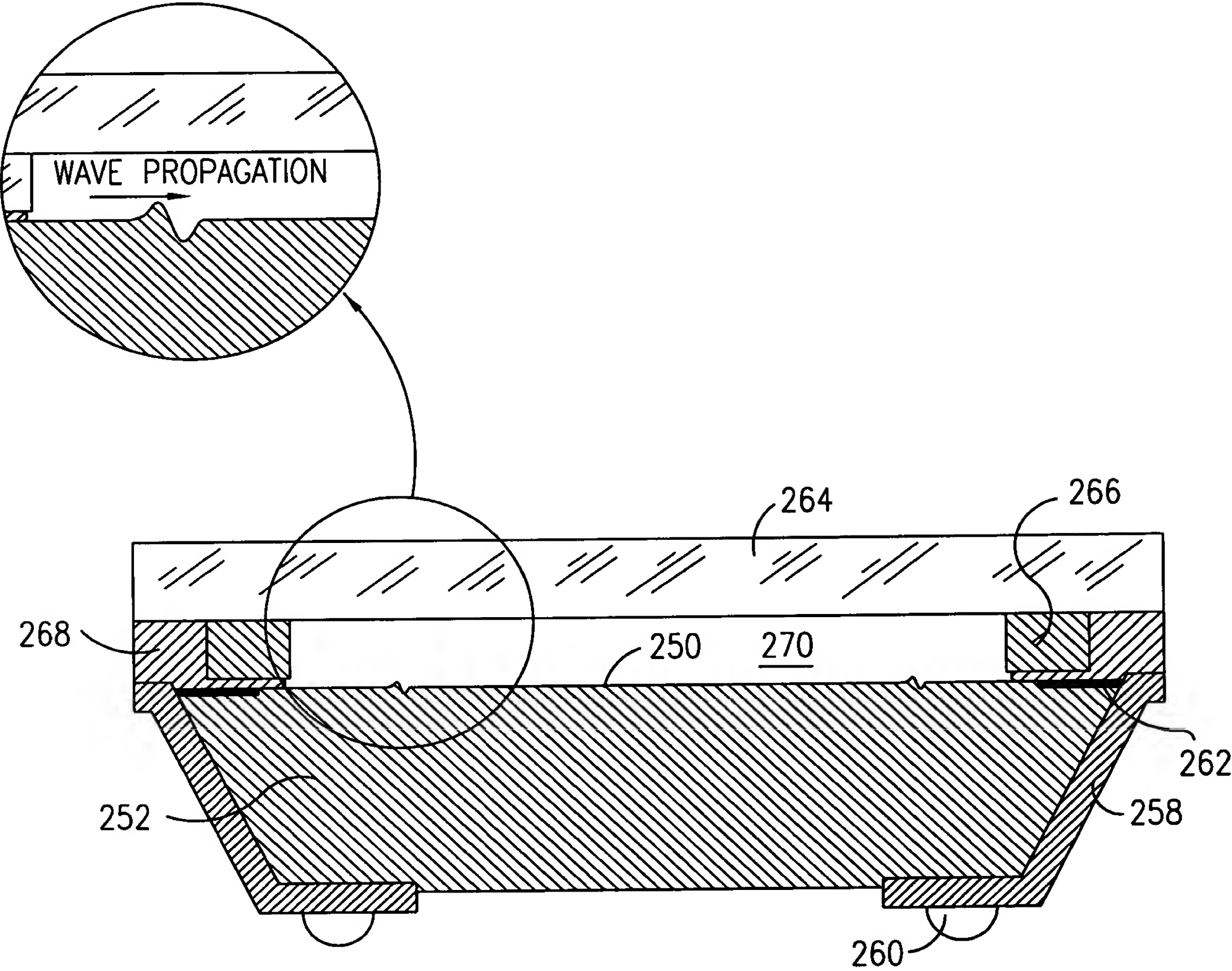


FIG. 3

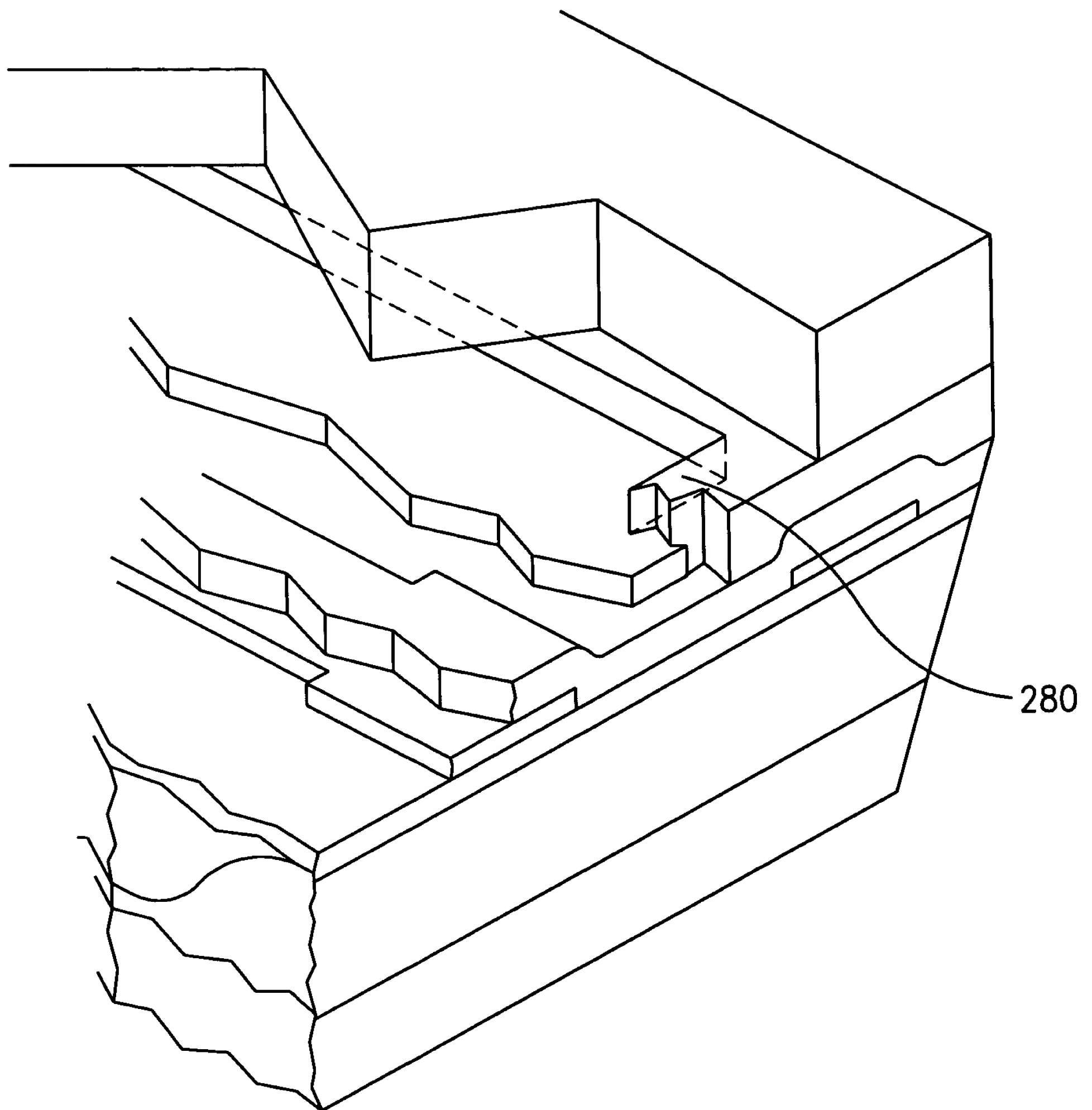


FIG. 4A

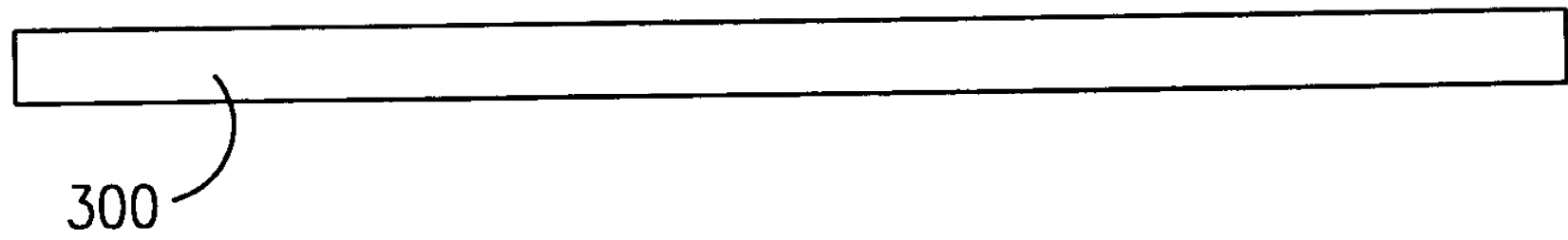


FIG. 4B

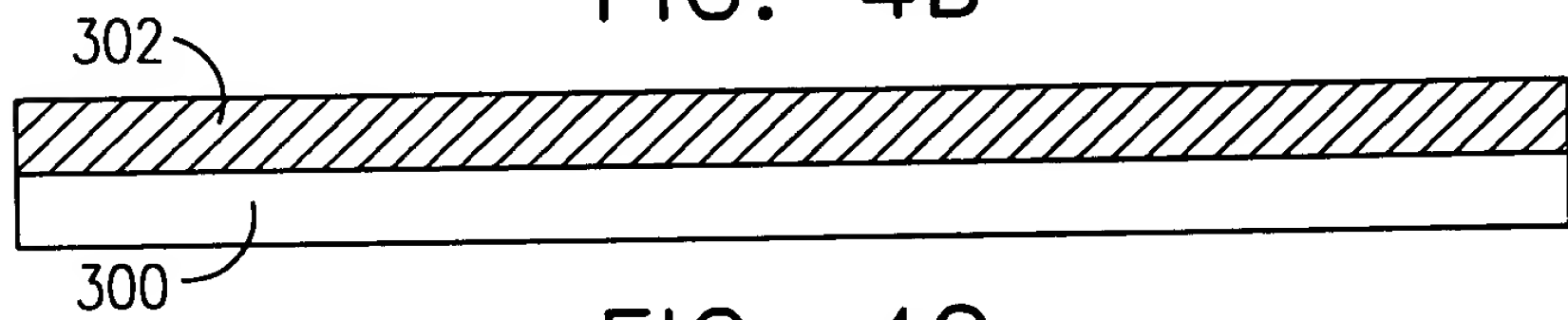


FIG. 4C

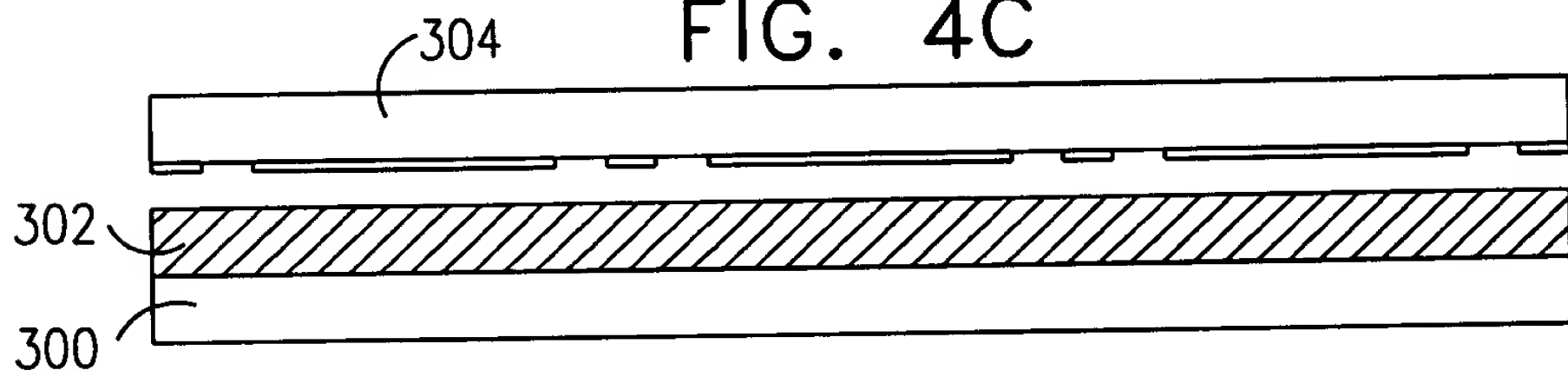


FIG. 4D

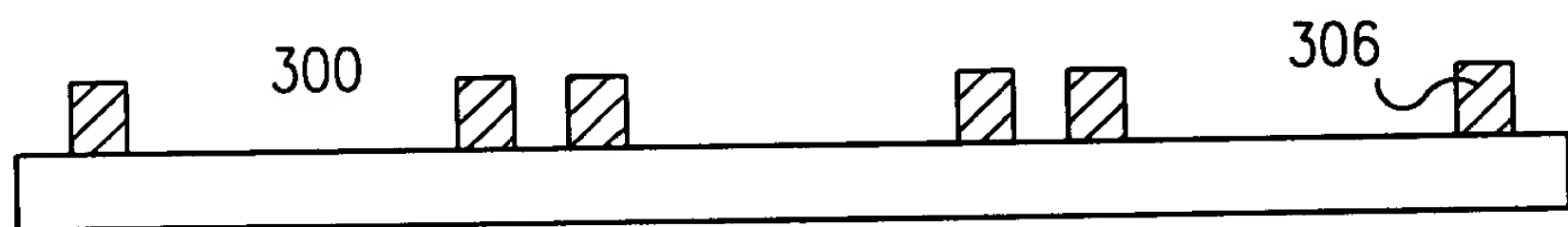


FIG. 4E

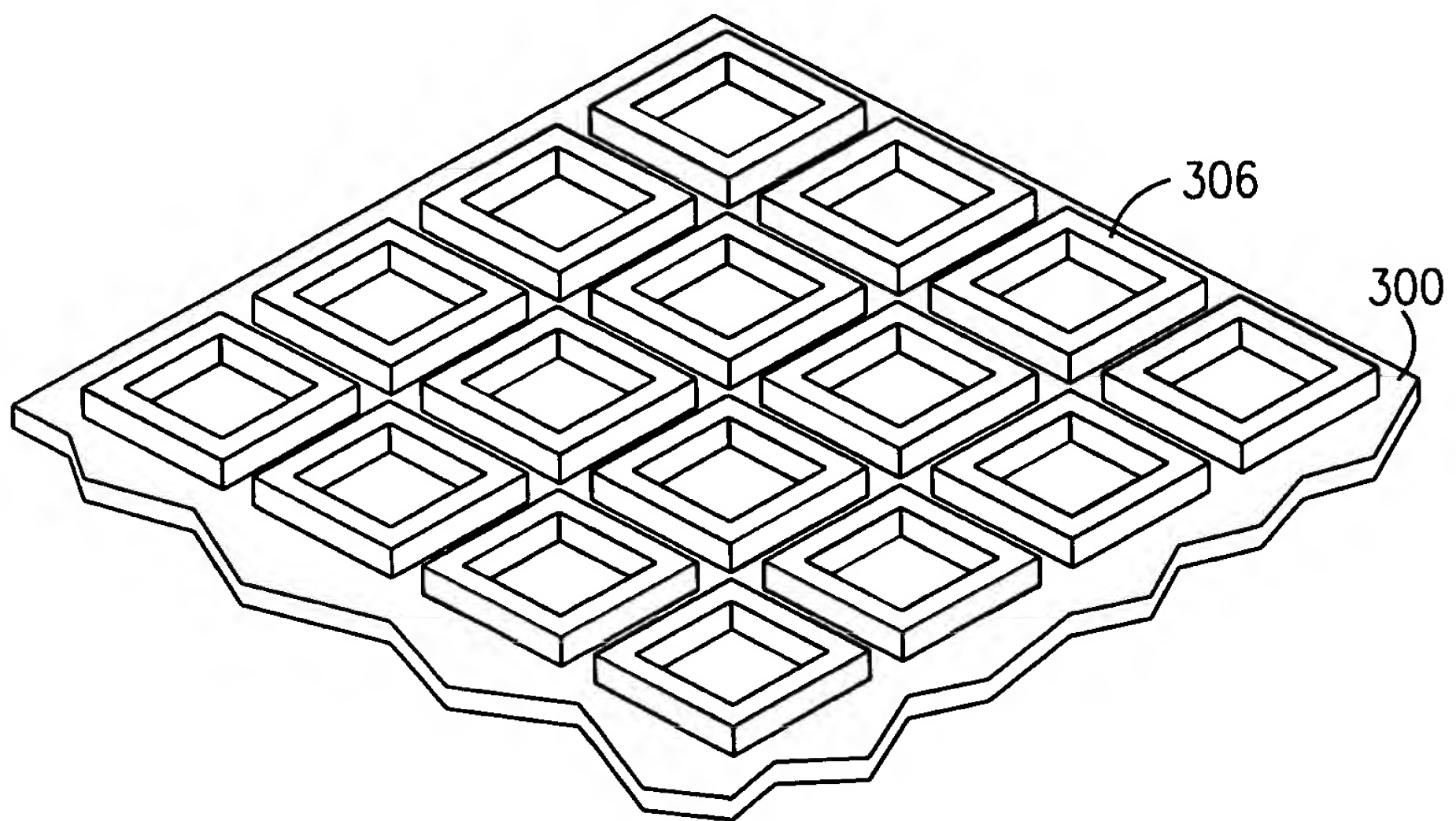


FIG. 5A

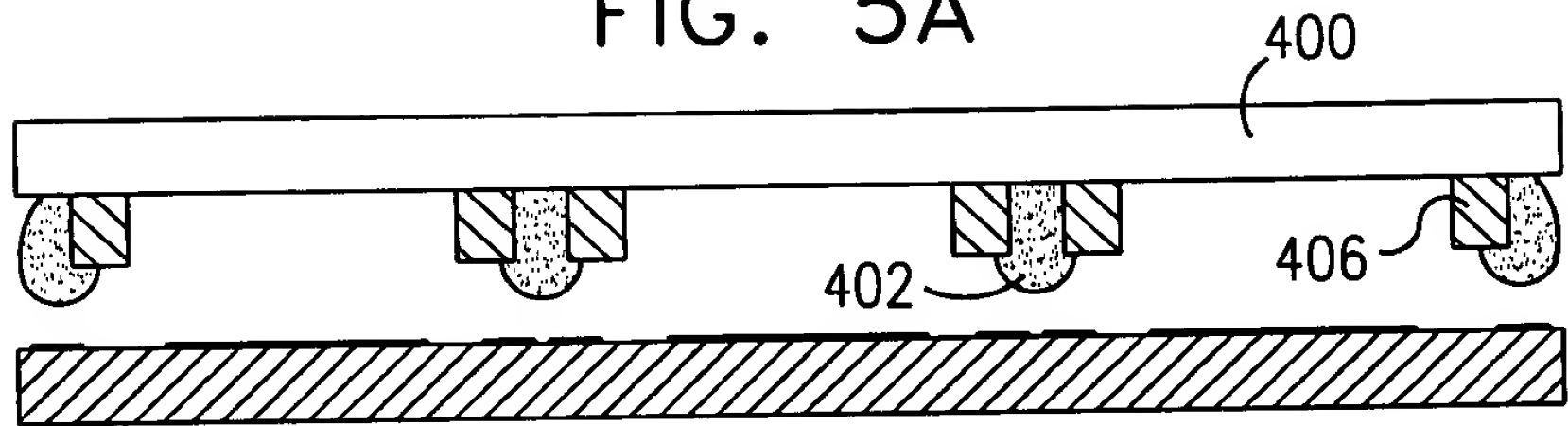


FIG. 5B

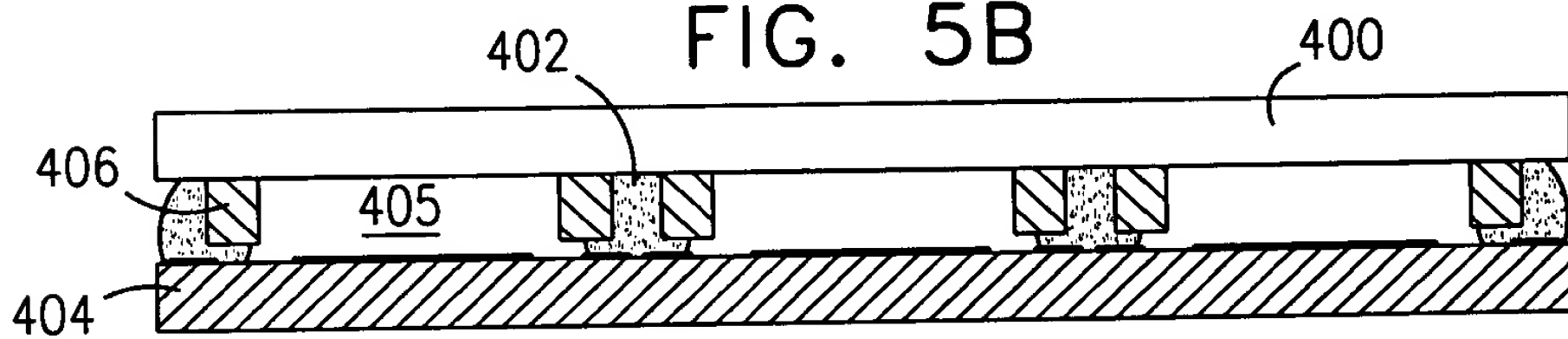


FIG. 5C

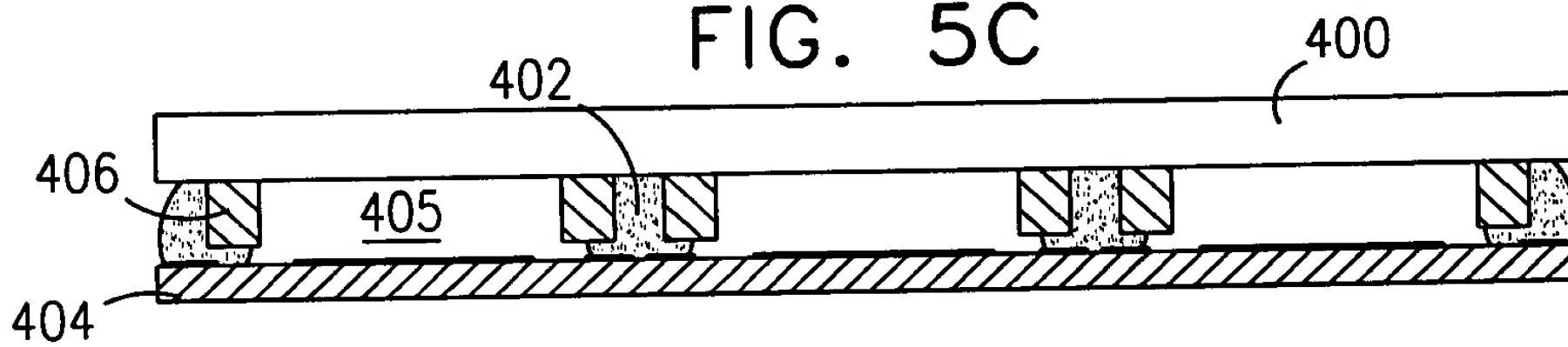


FIG. 5D

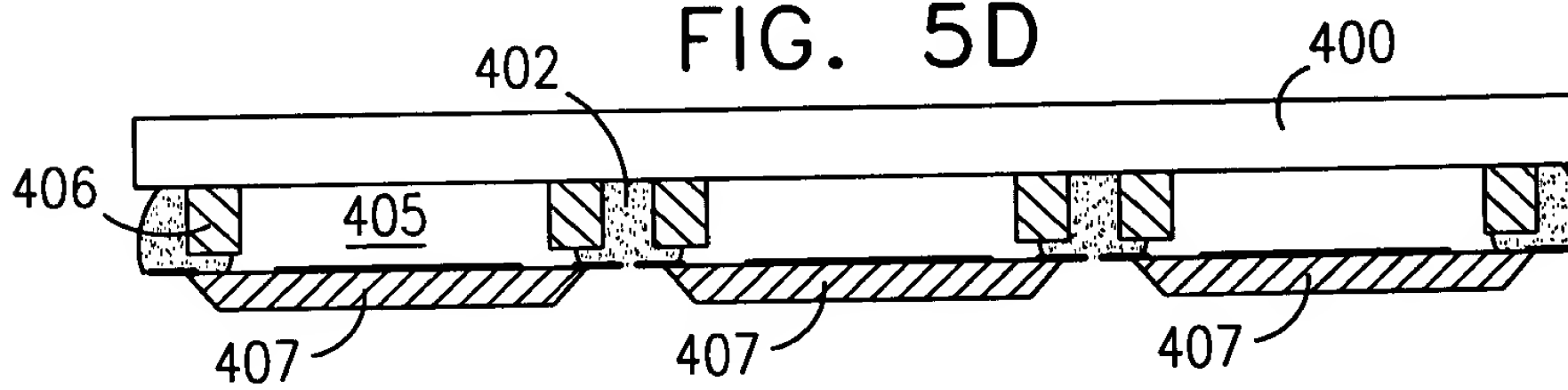


FIG. 5E

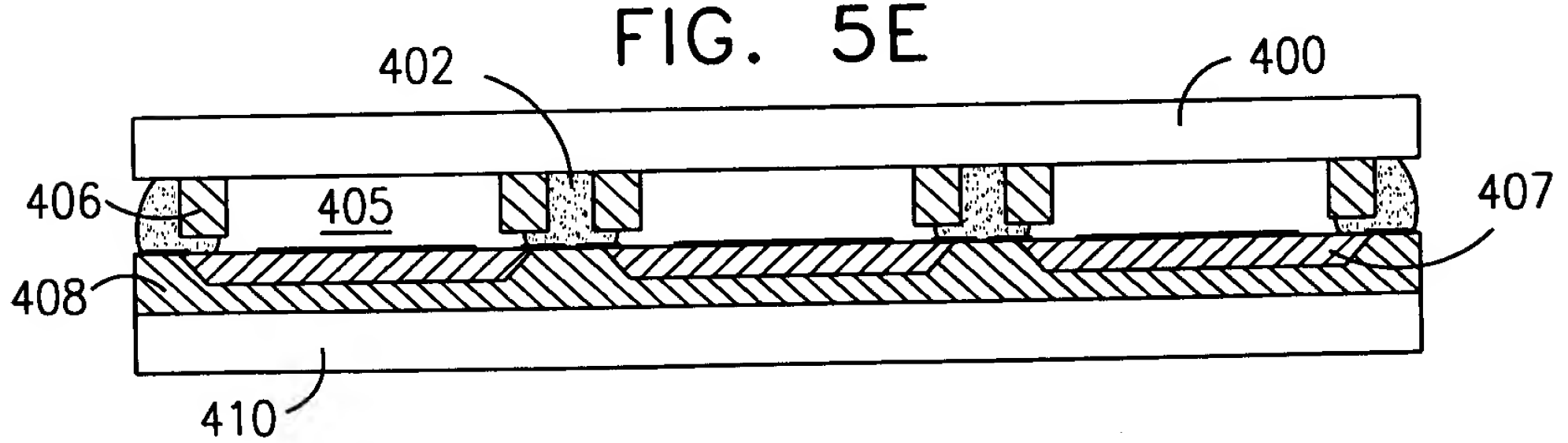
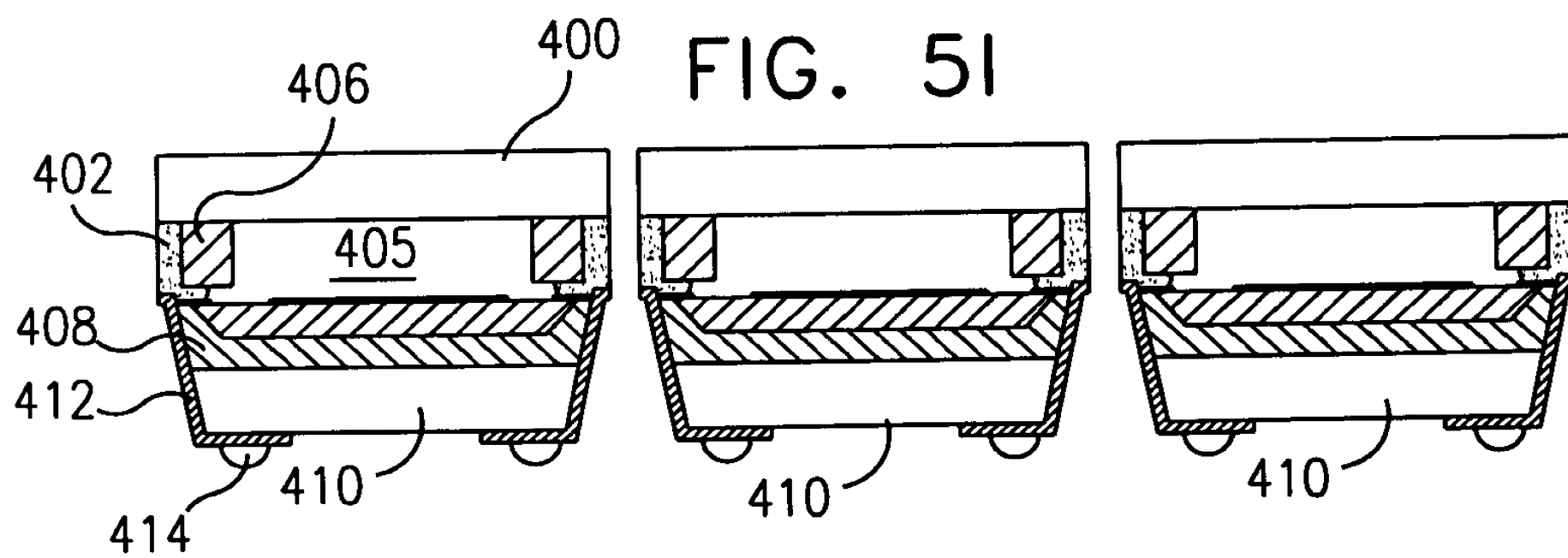
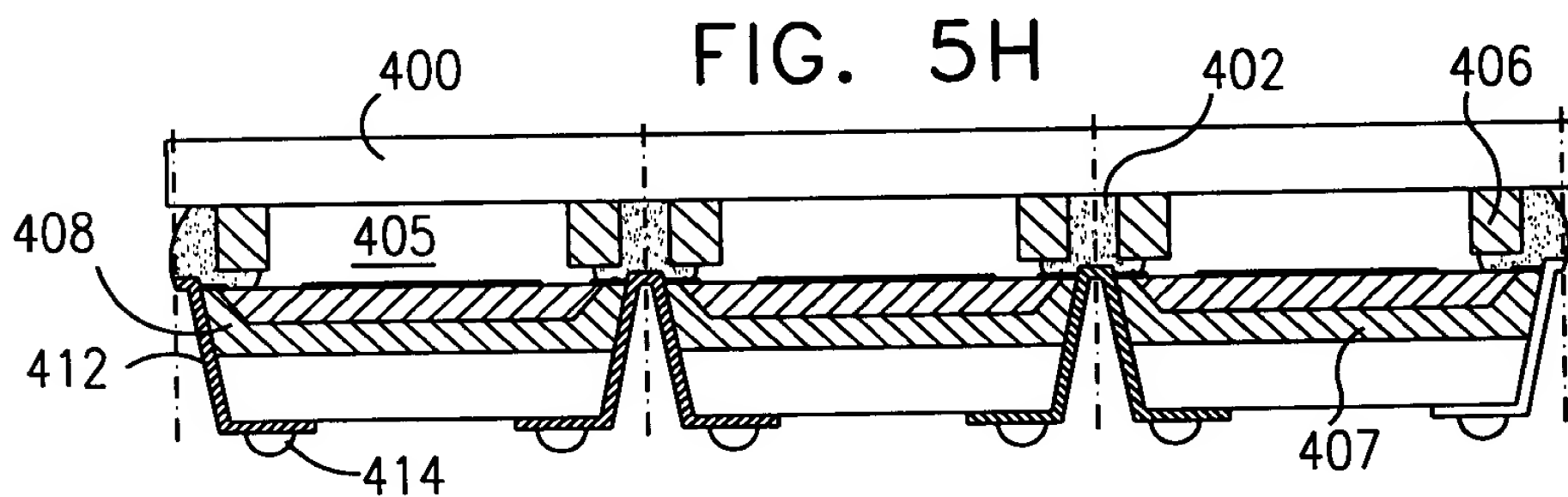
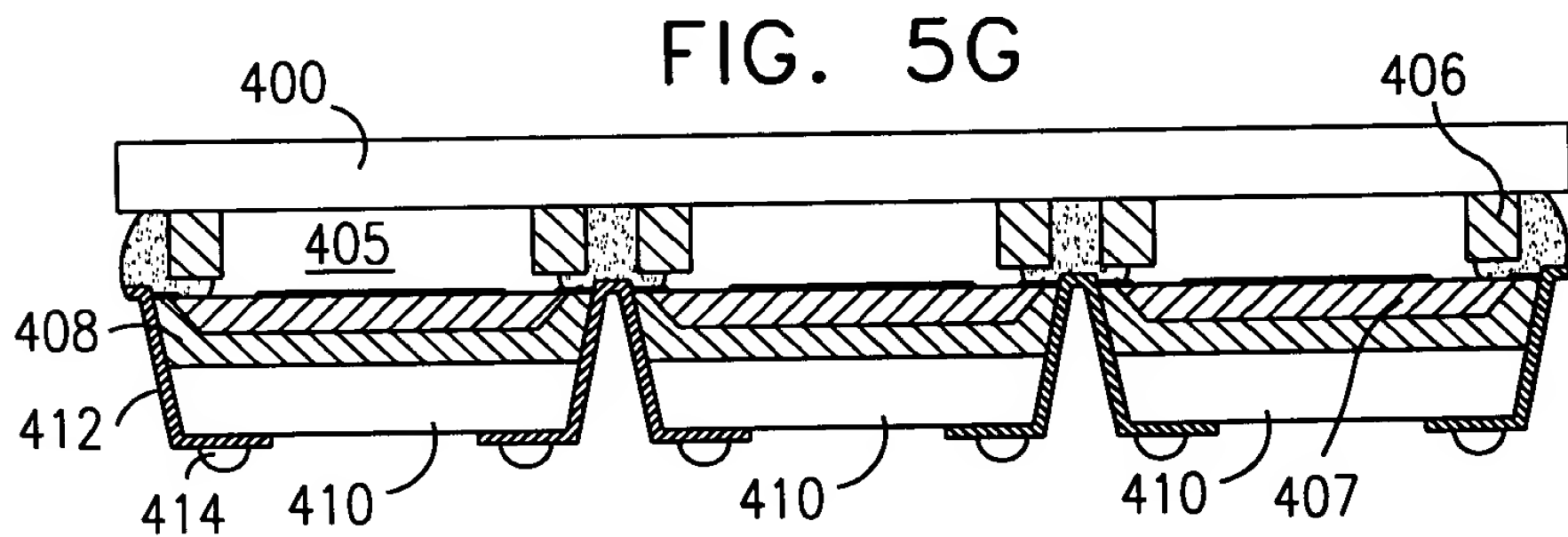
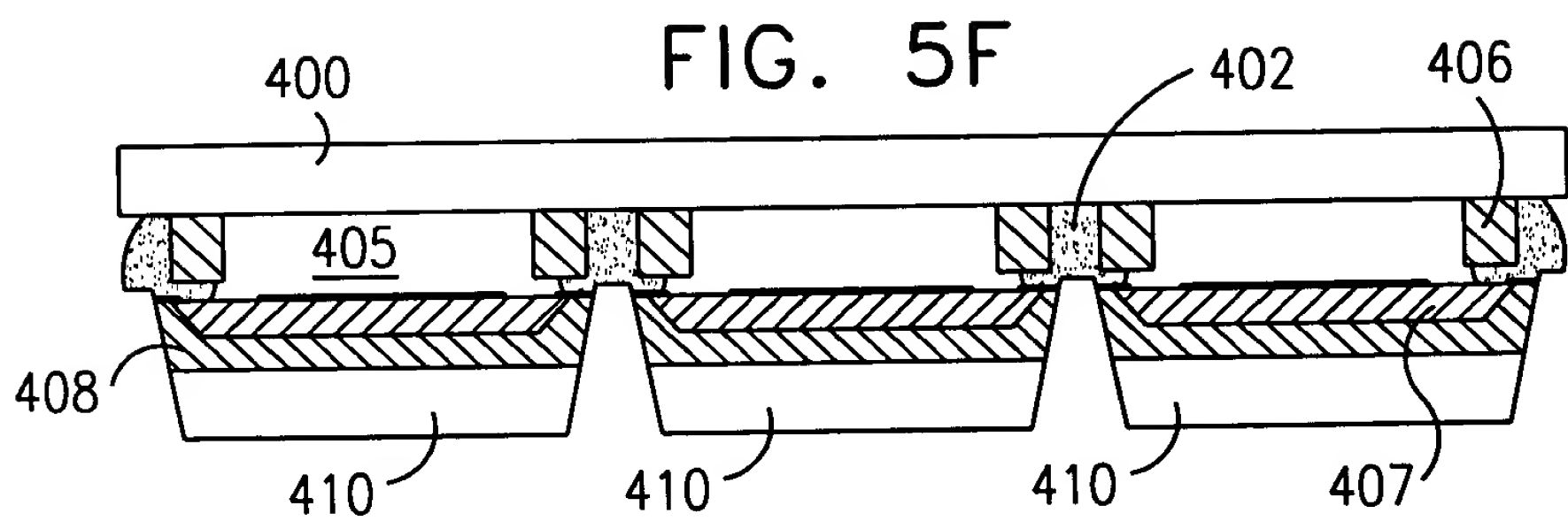


FIG. 5F





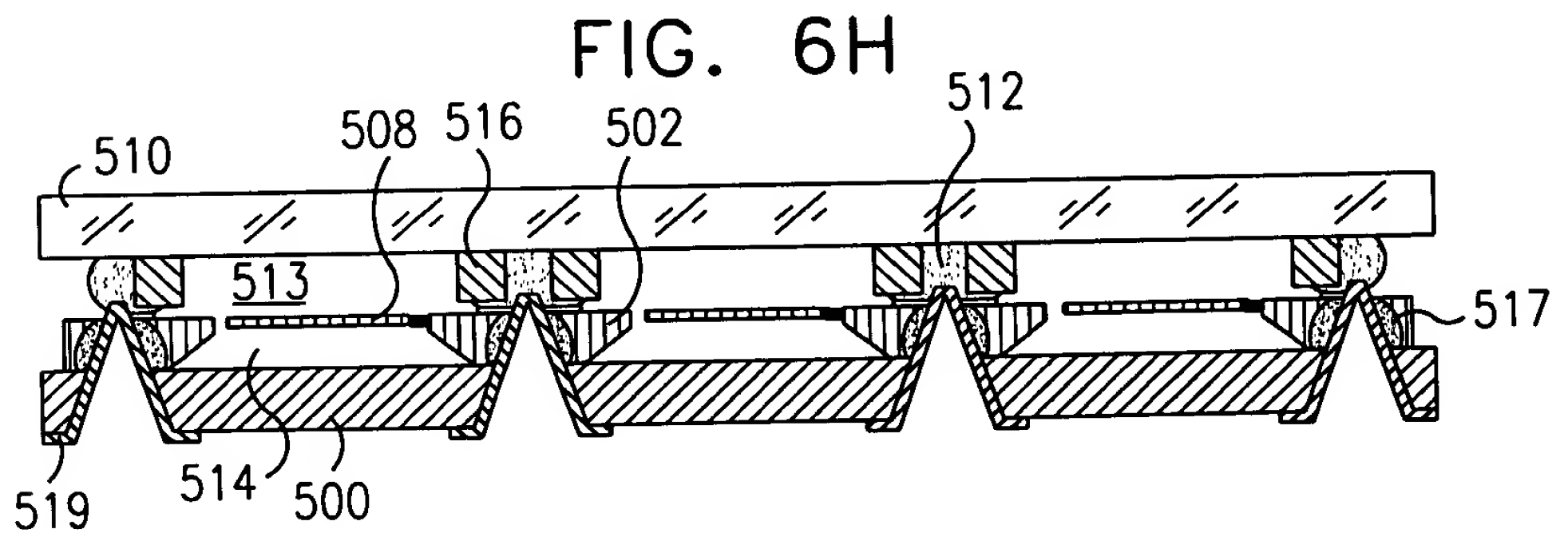
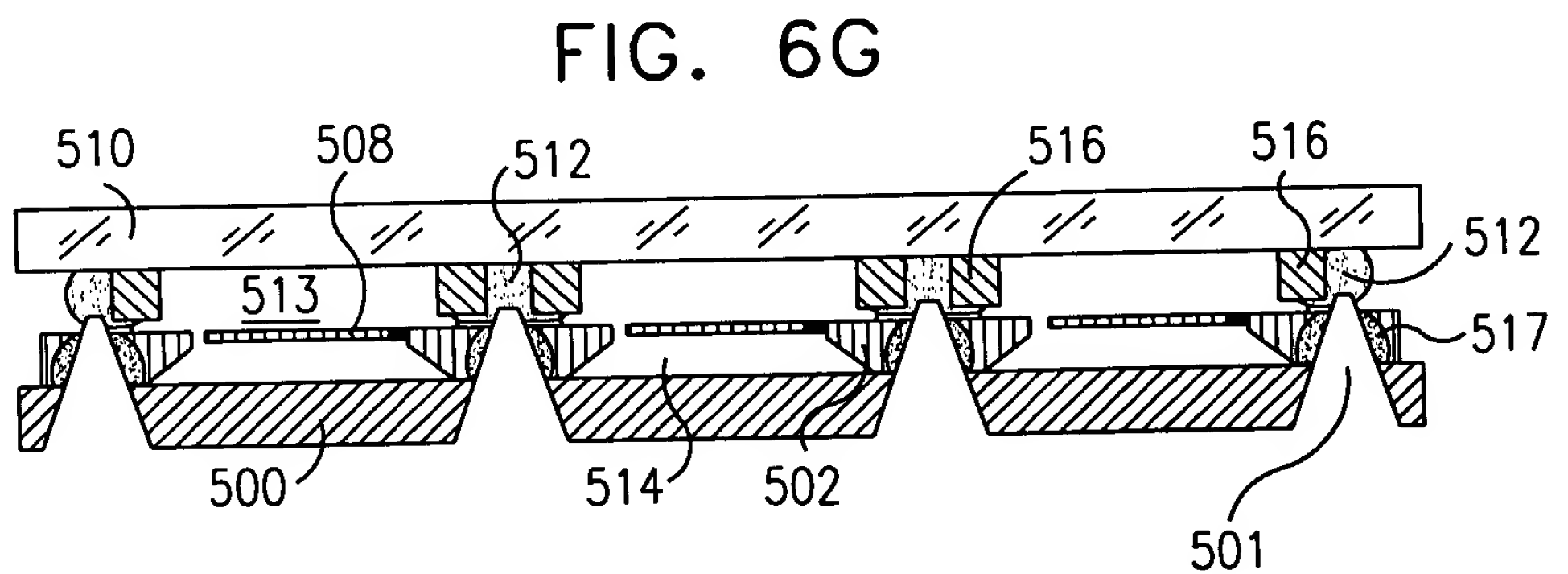
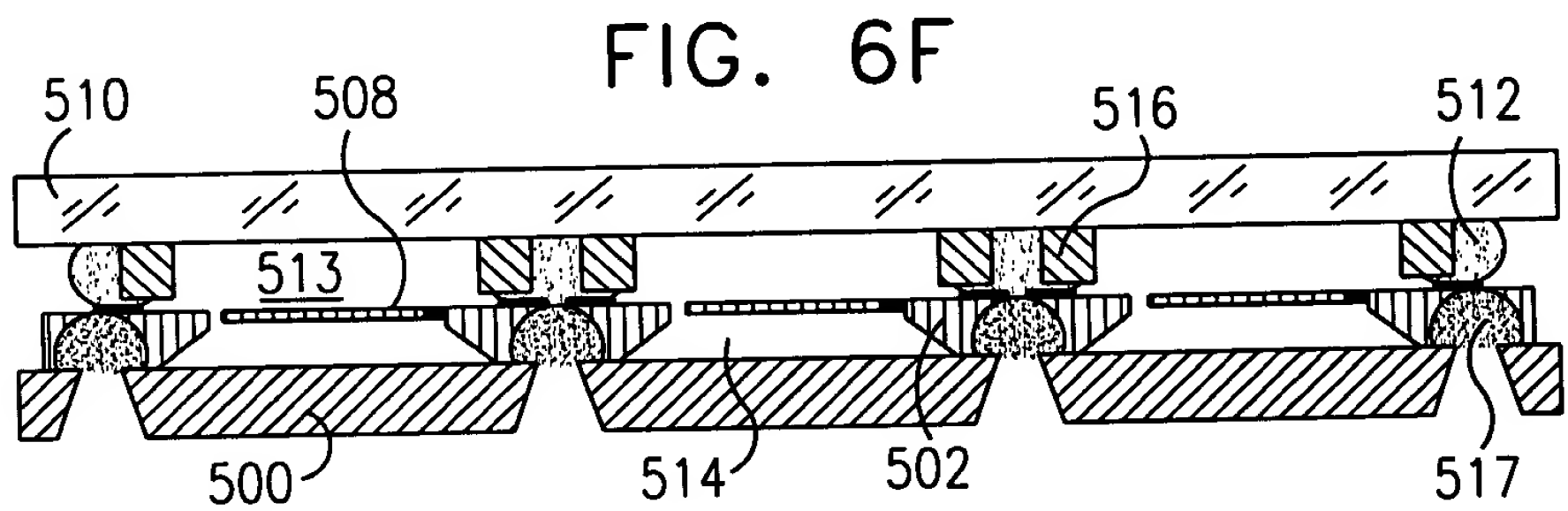
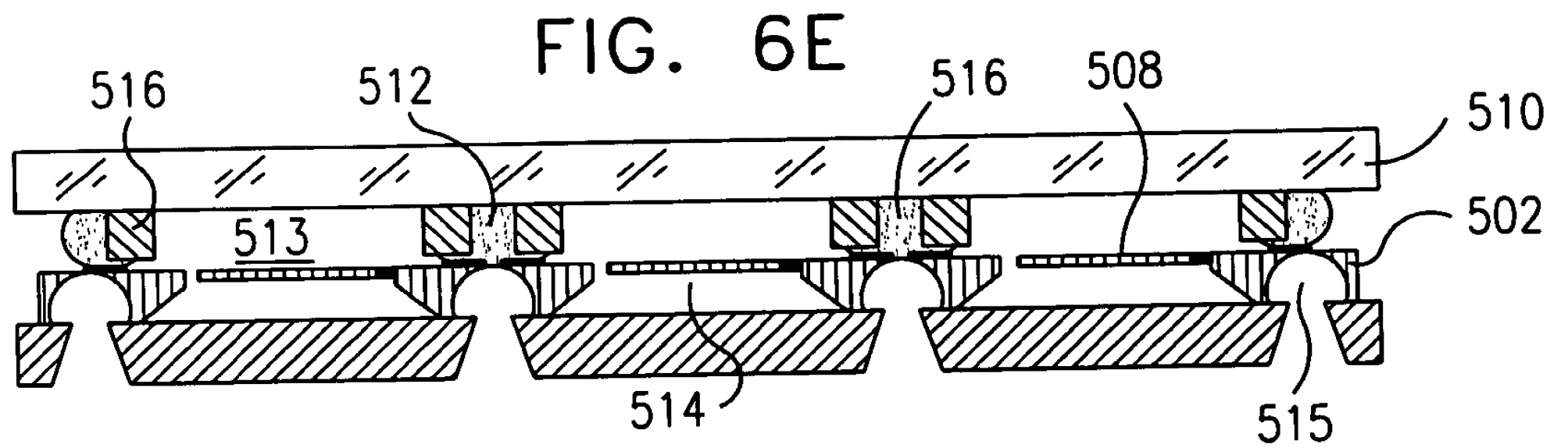
A cross-sectional view of a semiconductor device. A substrate 500 is shown at the bottom. A layer 502 is formed on the substrate. Various patterns are formed on the layer 502, including a pattern 504, a pattern 506, a pattern 508, and a pattern 502.



FIG. 8C

502, 504, 506, 508, 510, 513, 514, 500





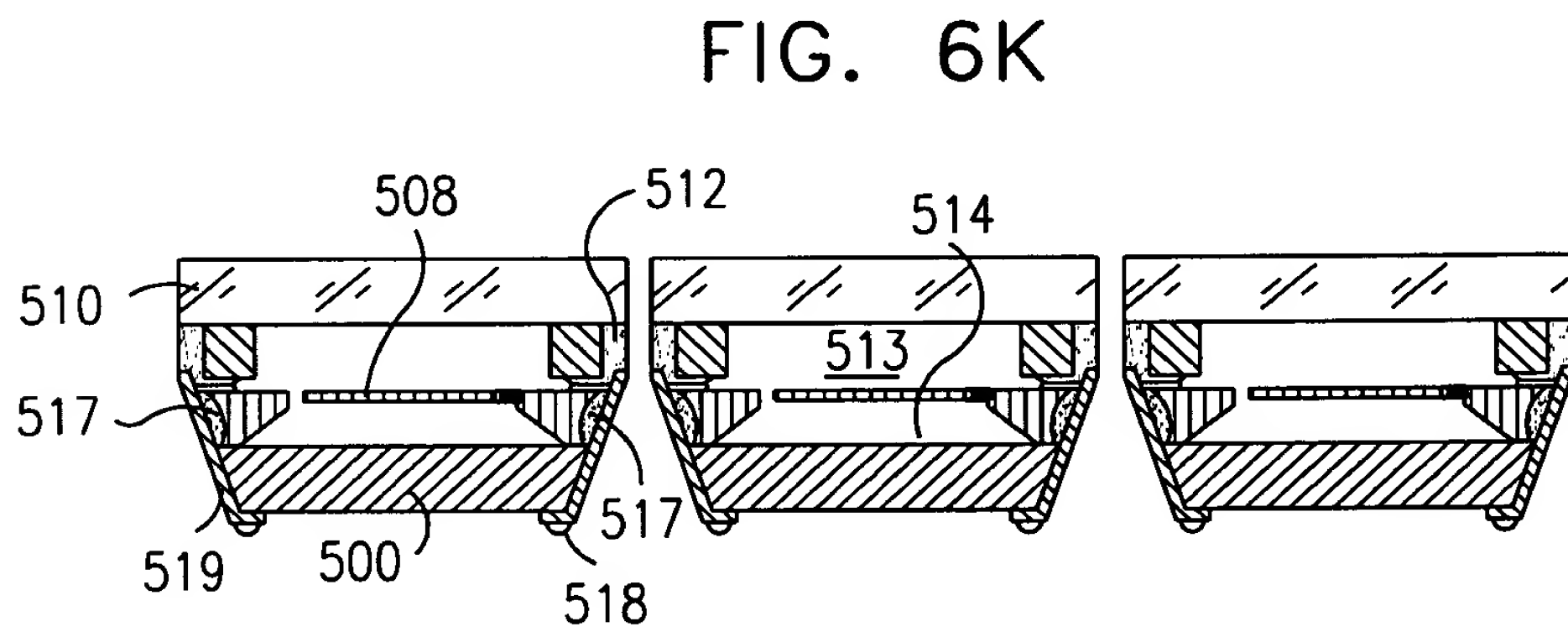
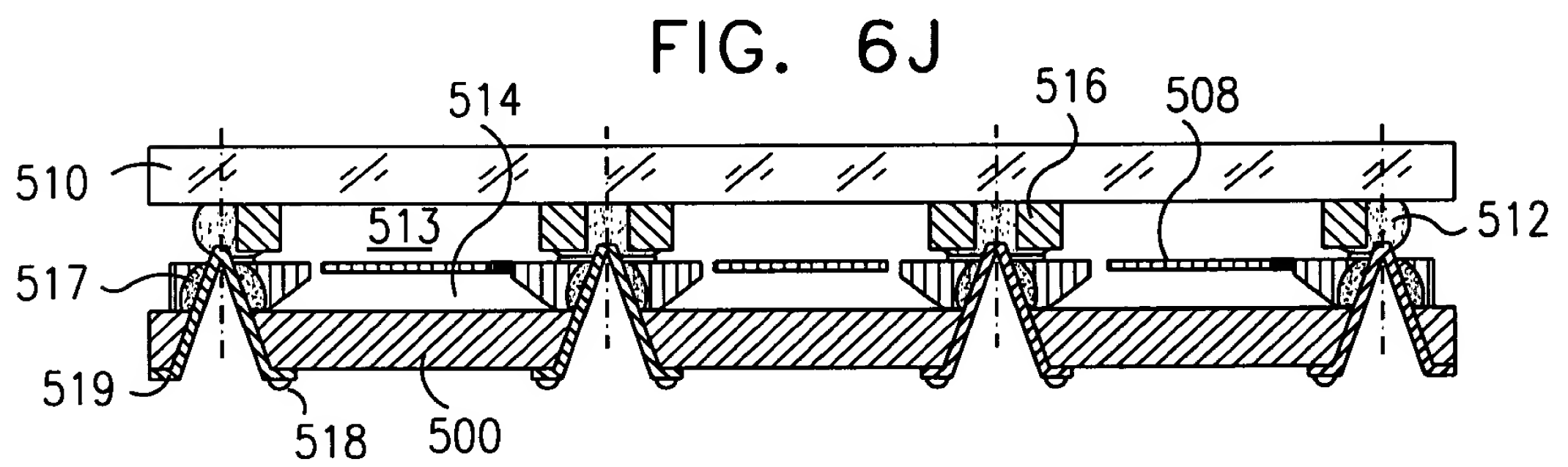
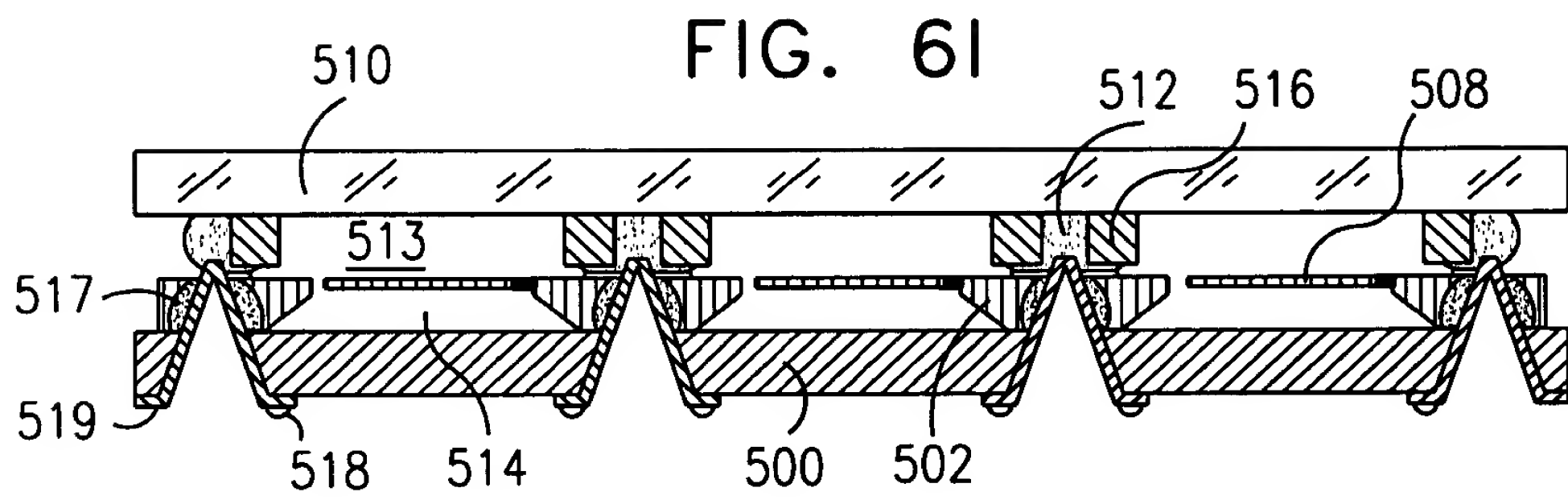


FIG. 7A

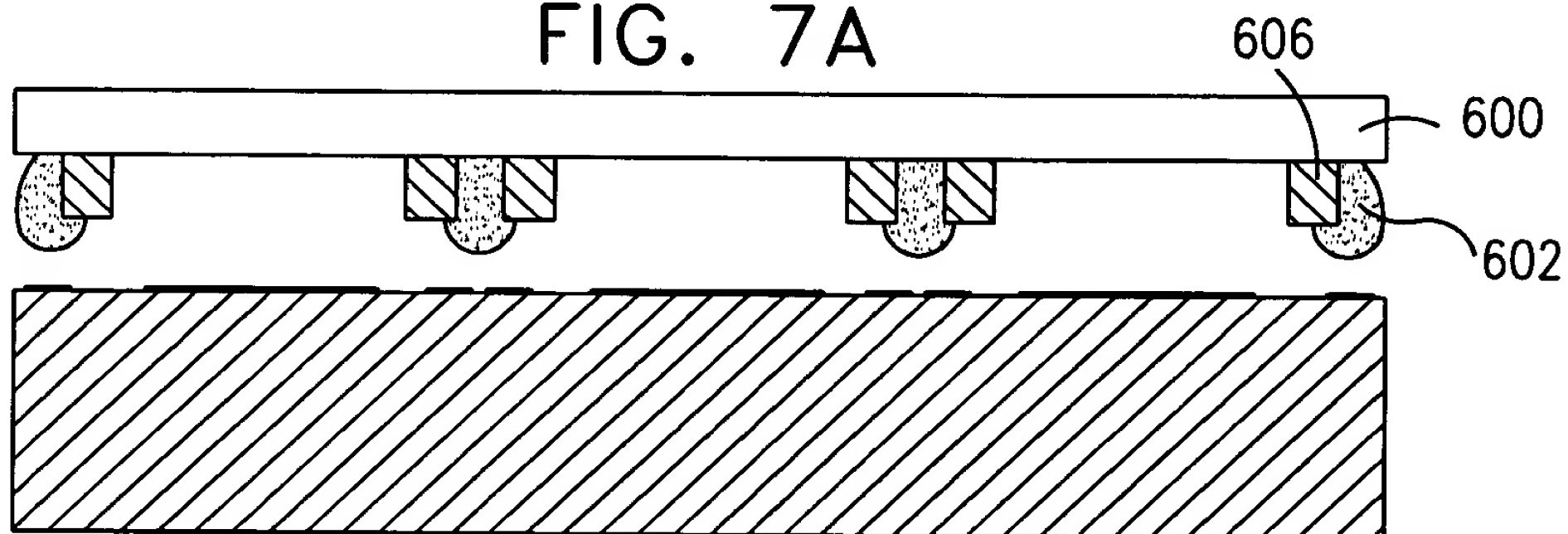


FIG. 7B

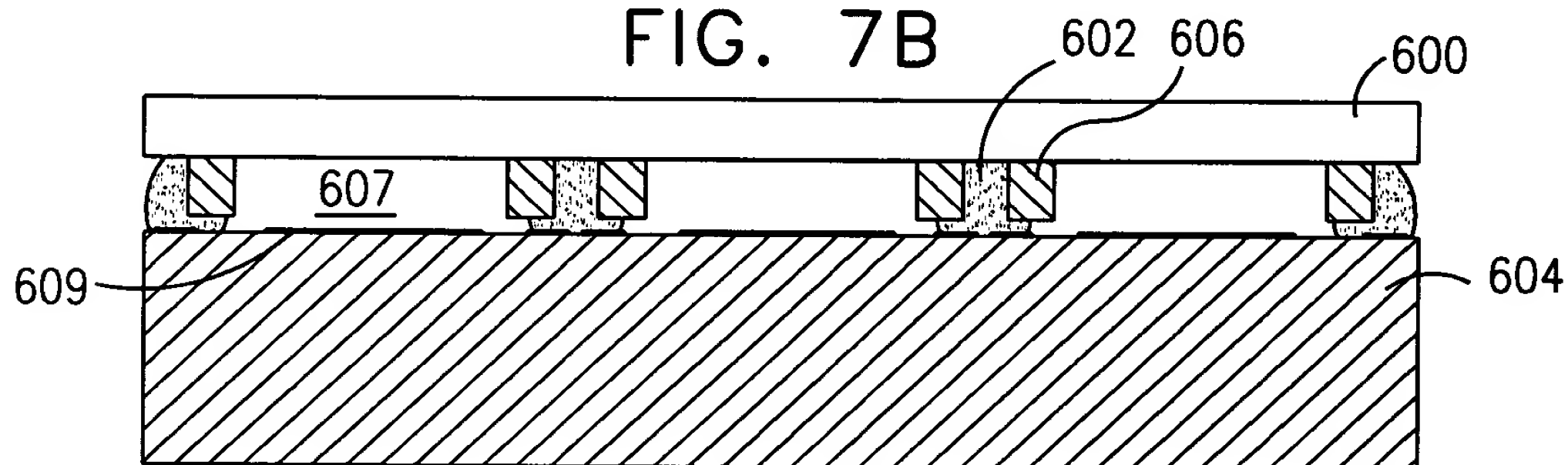


FIG. 7C

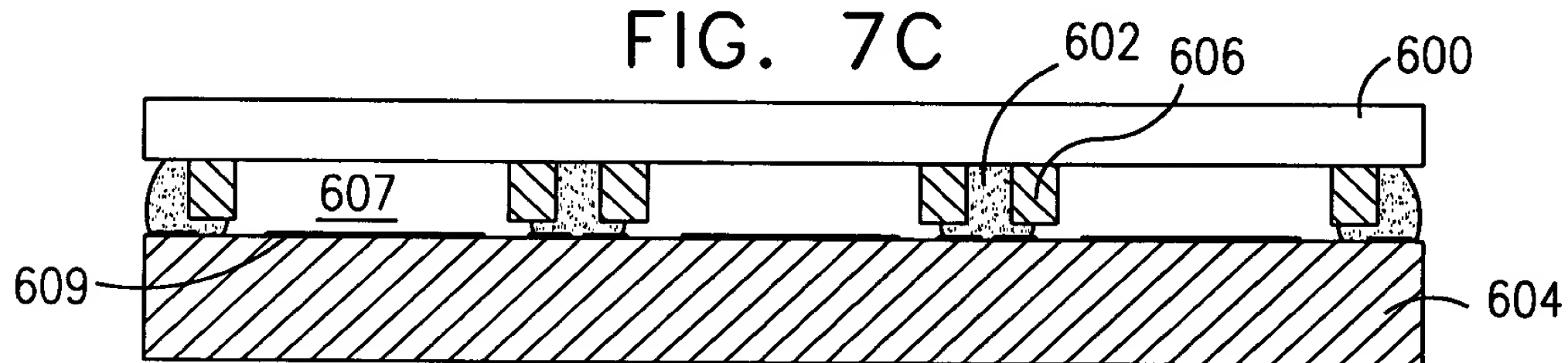


FIG. 7D

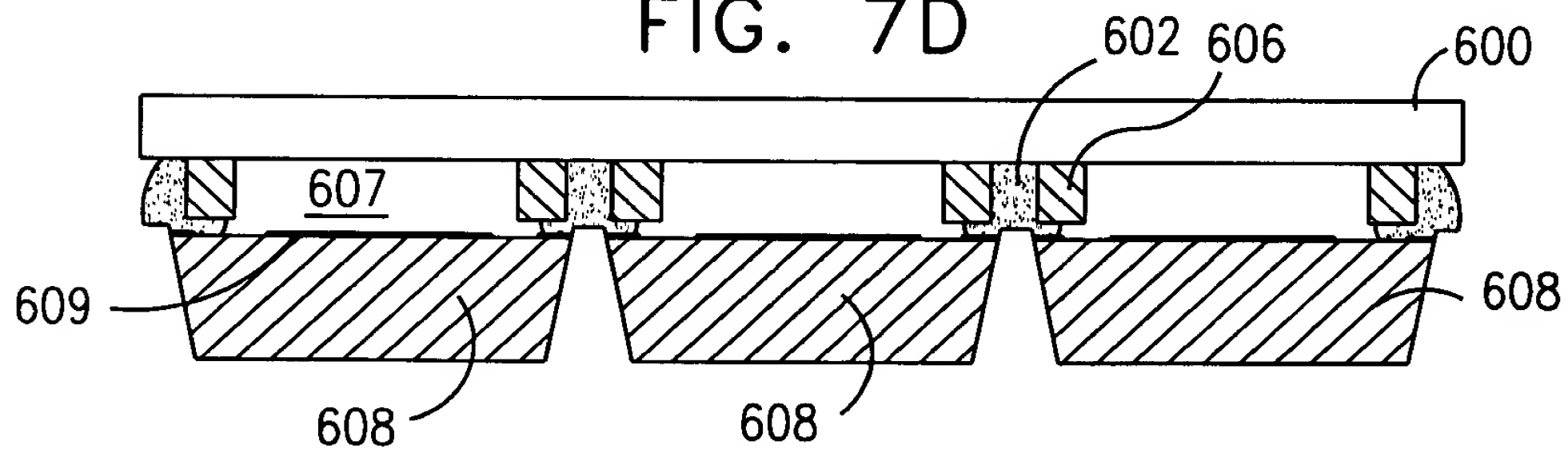


FIG. 7E

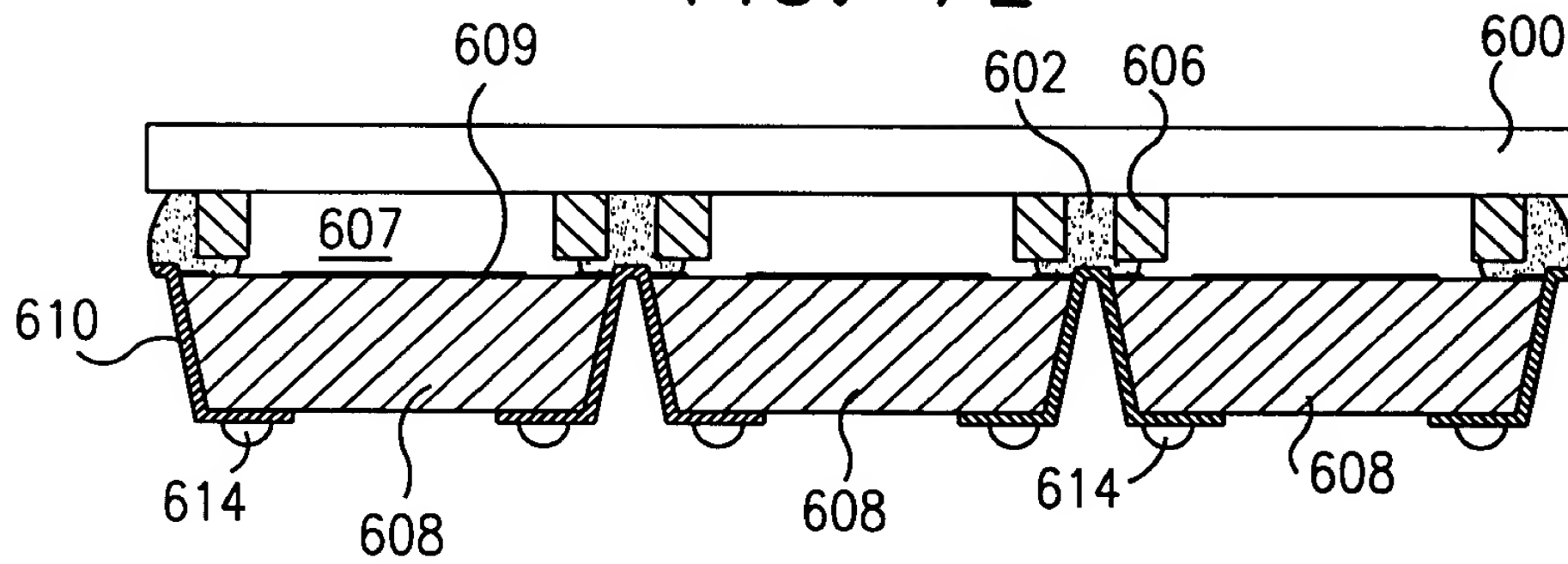


FIG. 7F

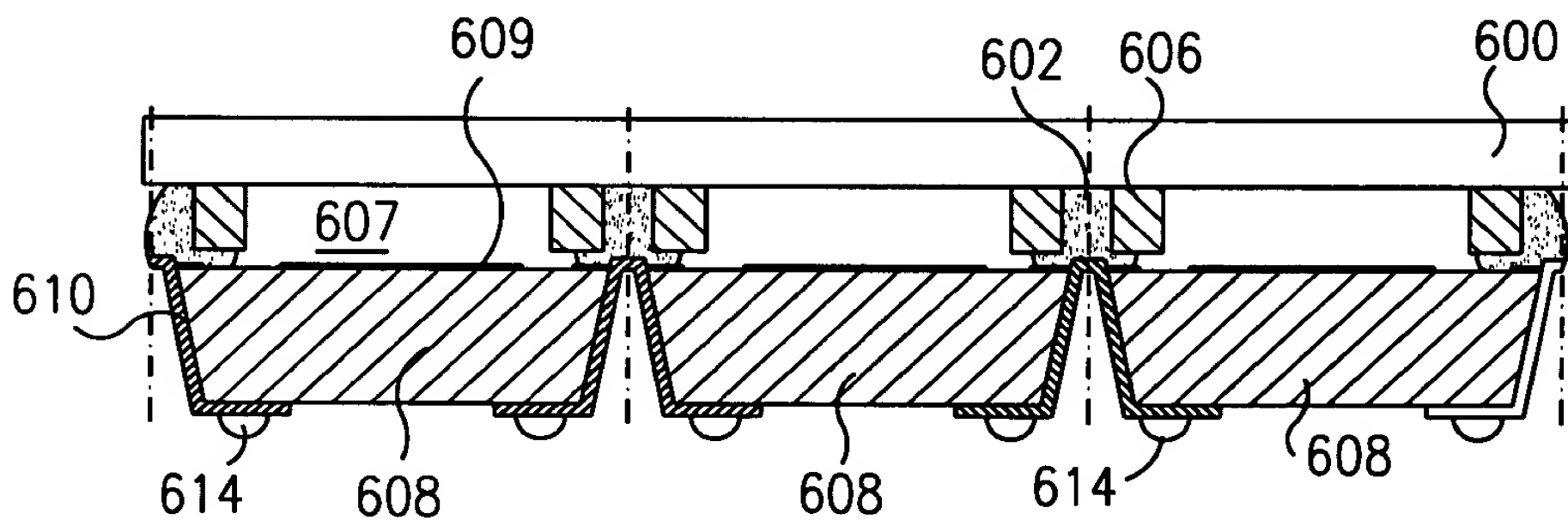
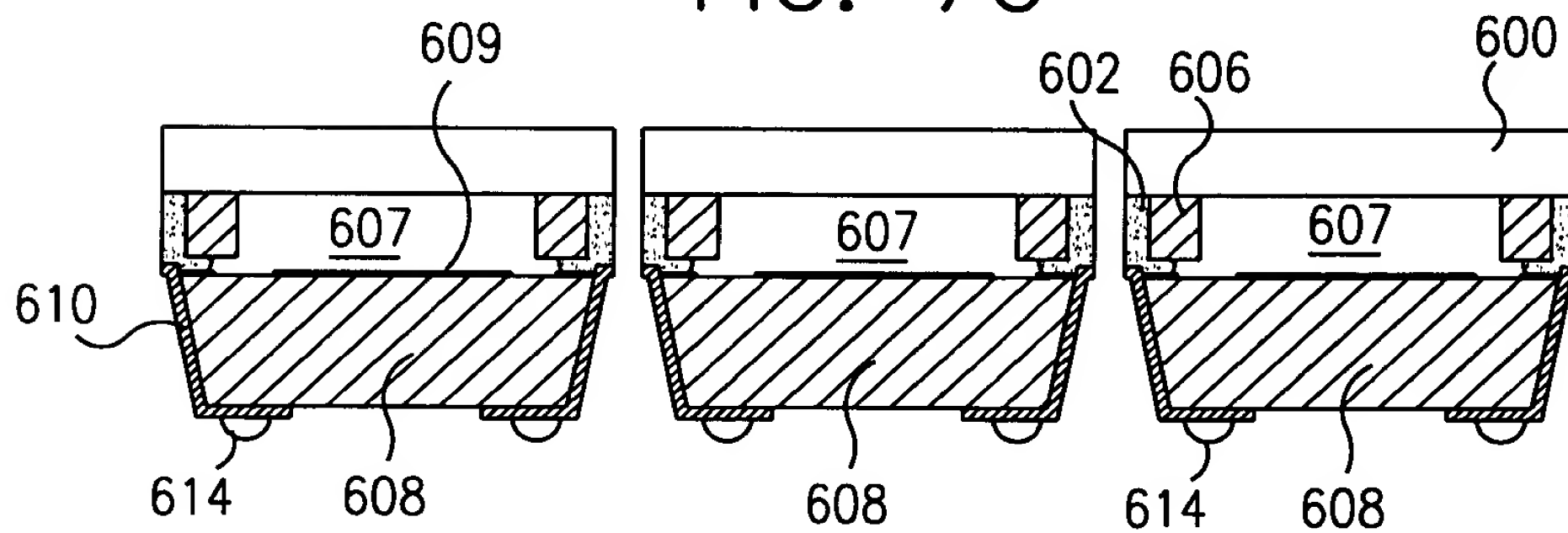


FIG. 7G



WAFER  
FABRICATION

FIG. 8A

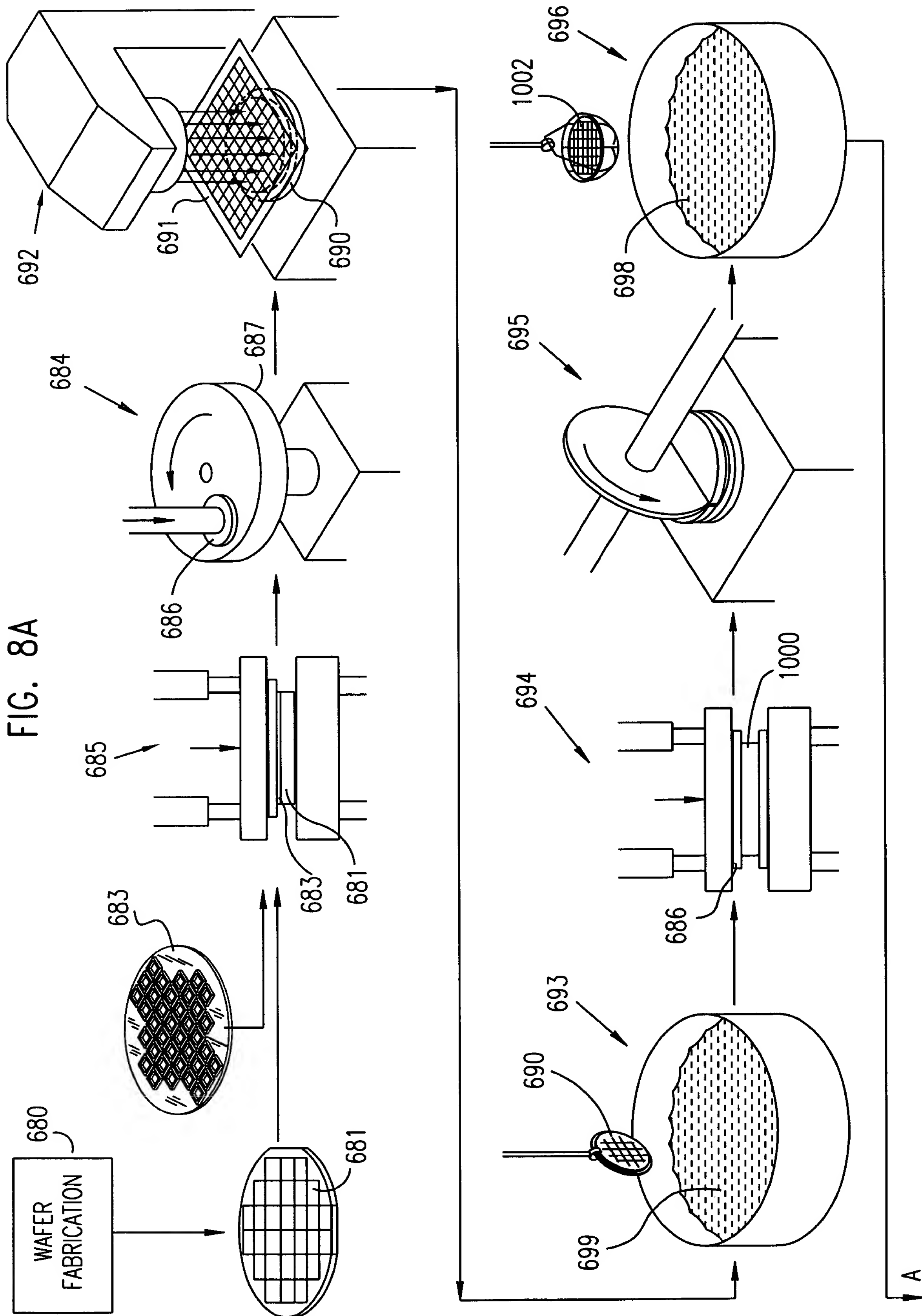


FIG. 8B

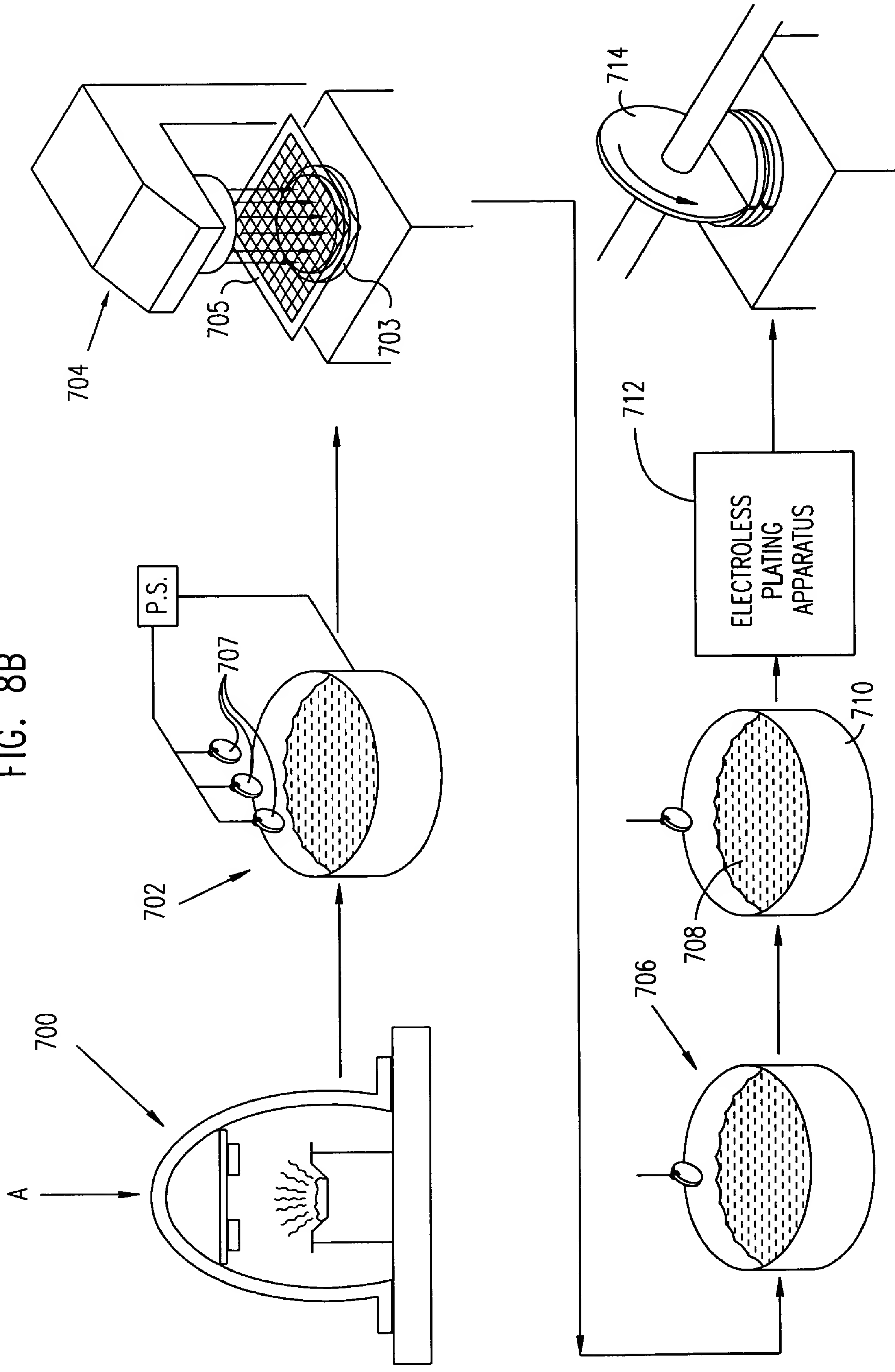


FIG. 9A

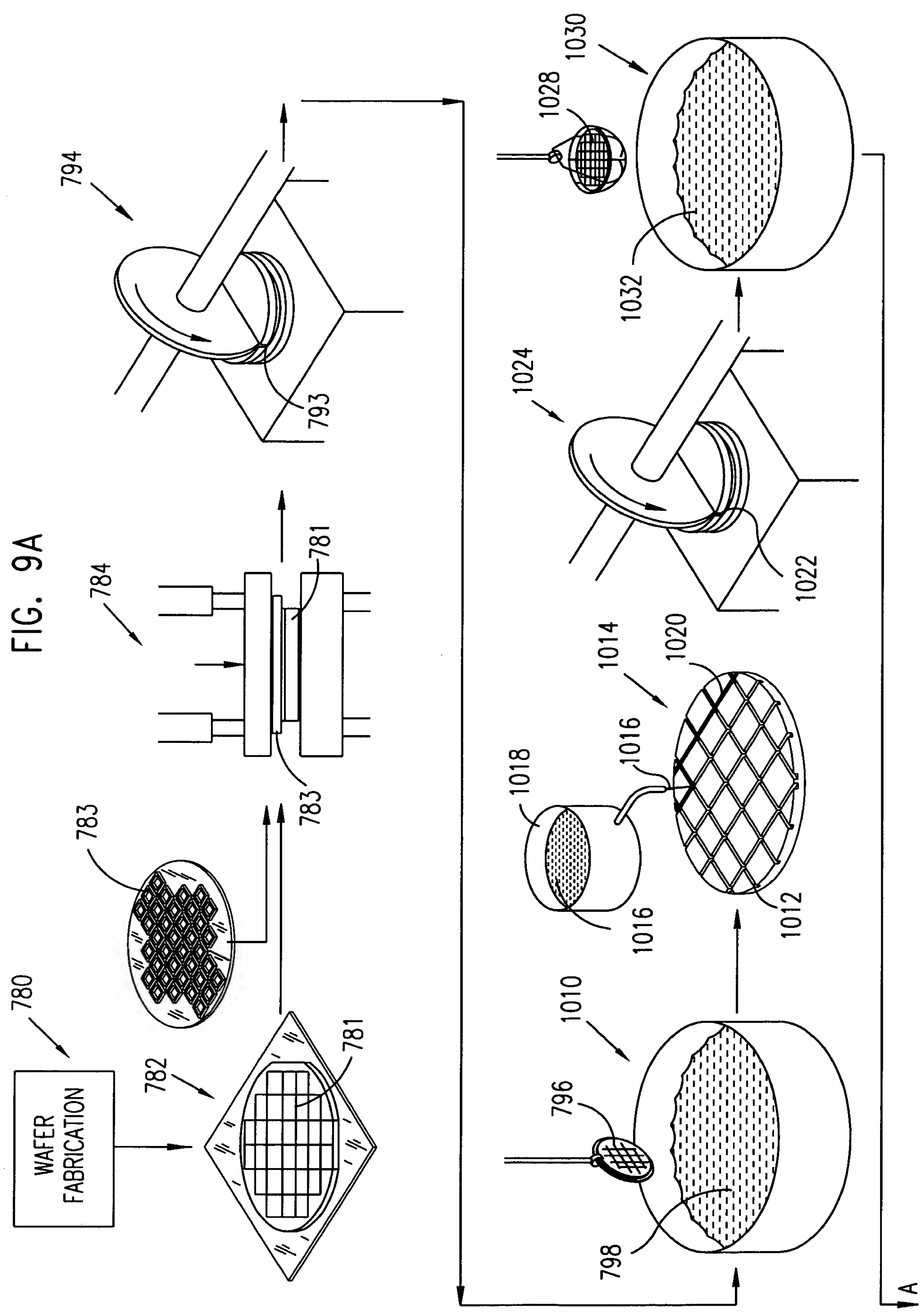
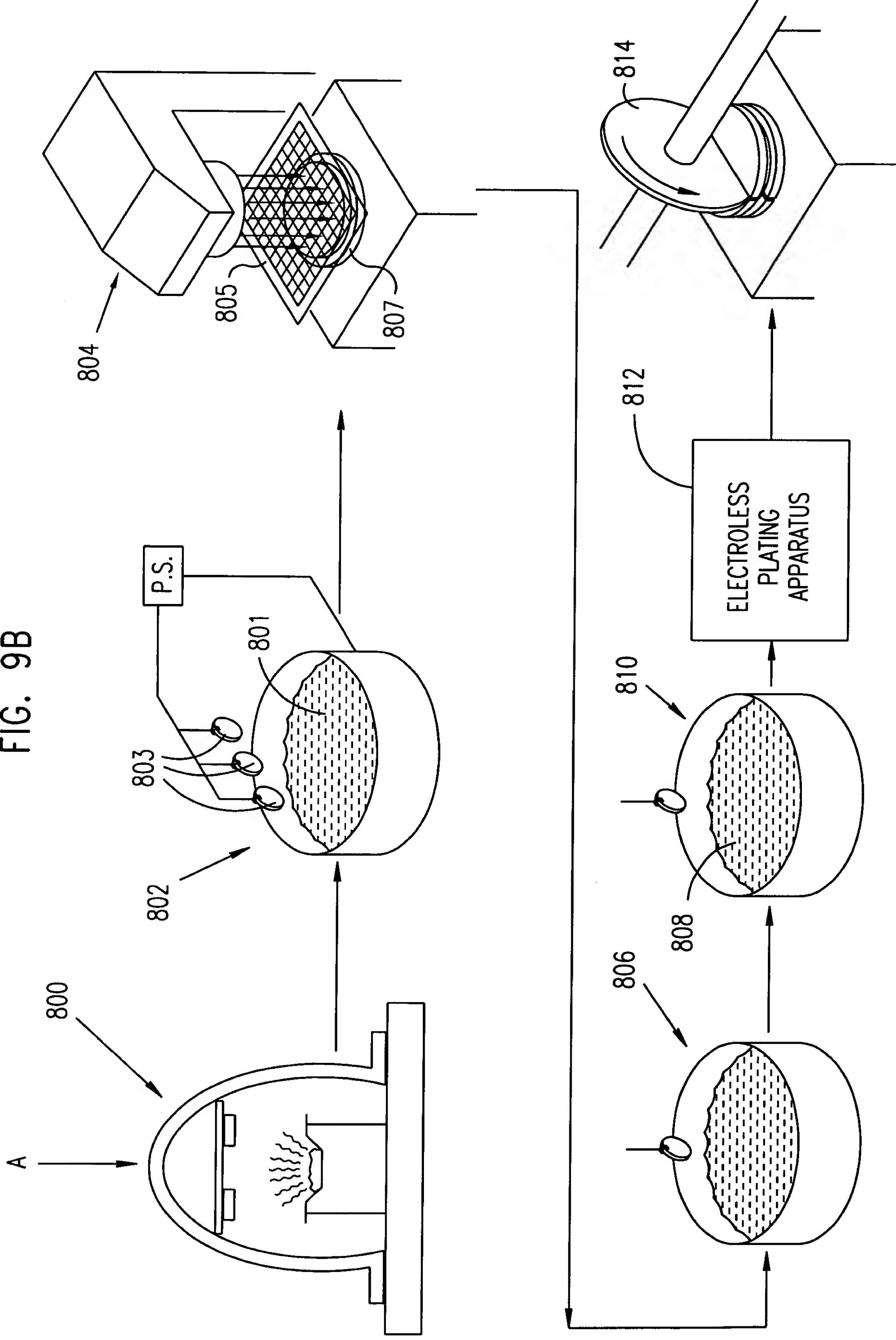




FIG. 9B



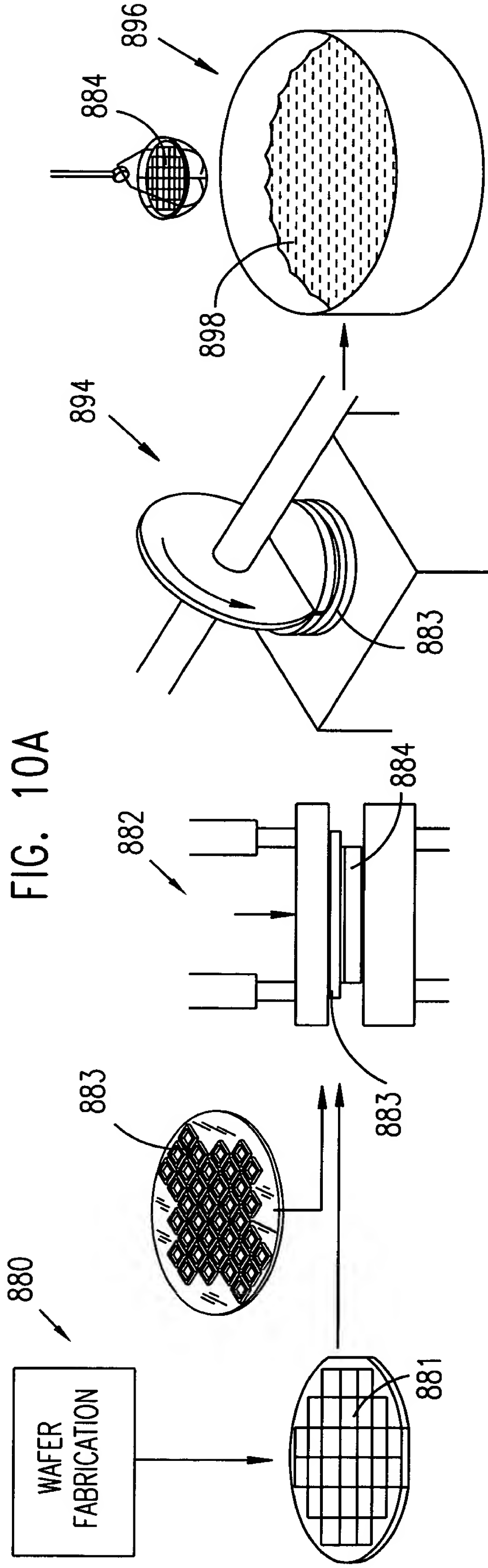


FIG. 10B

